IN THE CLAIMS:

Please substitute the following amended claims for like numbered claims in the existing application:

1. **(Original)** A method for tracking a CDMA pilot channel signal to discipline an oscillator, comprising:

downconverting an RF signal from a RF center frequency f_{RF} to an intermediate center frequency f_L where f_L is greater than or equal to a CDMA chip rate f_c, wherein downconverting includes incorporating bandpass filtering to remove extraneous signals while passing said CDMA pilot channel signal;

converting a signal format from analog to digital using a single analog-to-digital converter employing a sampling rate of f_s to create a digital signal $\{s(n)\}$;

employing a correlation circuit to establish a correlation between $\{s(n)\}$ and locally generated versions of I-channel and Q-channel PN signals, $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, respectively; and

generating an estimate of a frequency error of the oscillator using Correlation values corresponding to (2M+1) time shifts of $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, the (2M+1) time shifts being $K-\Delta_M$, $K-\Delta_{(M-1)}$, . . . , $K-\Delta_2$, $K-\Delta_1$, K, and $K+\Delta_1$, $K+\Delta_2$, . . . , $K+\Delta_{(M-1)}$, $K+\Delta_M$, where a time shift of K corresponds to a time shift that provides the maximum correlation value, and M is greater than or equal to 1.

2. **(Original)** The method of claim 1, wherein the sampling rate, f_s, the intermediate center frequency, f_L, and the chip rate f_c, are related by $f_s=4f_c$, and $f_L=f_c+kf_s$ for k=0.

3. **(Original)** The method of claim 1, wherein the sampling rate, f_s, the intermediate

center frequency, f_L, and the chip rate f_c, are related by $f_s = 4f_c$, and $f_L = f_c + kf_s$ for k=1.

4. **(Original)** The method of claim 1, wherein the sampling rate, f_s, the intermediate center frequency, f_L, and the chip rate f_c, are related by $f_s = 4f_c$, and $f_L = f_c + kf_s$ for k=2.

5. **(Original)** The method of any of claims 2-4, wherein the correlation circuit uses a single accumulator for generating both an in-phase ("real") part and a quadrature ("imaginary") part of a complex correlation between the digital signal $\{s(n)\}$ and a given time shifted version of the locally generated versions of $\{I_{PN}(n)\}$and $\{Q_{PN}(n)\}$.

6. **(Original)** The method of claim 5, wherein both positive overflows and negative underflows are monitored.

7. **(Original)** The method of claim 1, wherein a matched filter is not employed.

8. **(Original)** A receiver for performing the method of claim 1.

9. **(Original)** The method of claim 1, wherein the correlations are computed at time shift lags which are commensurate with the sampling rate.

10. **(Original)** The method of claim 9, wherein the correlations for lags smaller than the sampling interval are synthesized using a digital signal processing.

11. **(Original)** A receiver for performing the method of claim 1, further comprising an autonomous background correlator.

12. **(Original)** A receiver for performing the method of claim 1, further comprising an autonomous background correlator computing correlations over a period less than the time period of the PN signals.

13. **(Original)** A receiver for performing the method of claim 1 wherein correlation values for a lag are averaged over multiple periods of the PN signals.

14. **(Original)** An apparatus to track a pilot signal, comprising:

a correlator circuit adapted to compute a complex correlation between a received version of the pilot signal and locally generated versions of I-channel and Q-channel PN signals, $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, respectively.

15. **(Original)** The apparatus of claim 14, wherein said correlator circuit includes an FPGA.

16. **(Original)** The apparatus of claim 14, wherein the correlator circuit includes a single accumulator that computes both the real and imaginary part of the complex correlation.

17. **(Original)** The apparatus of claim 14, further comprising a signal processor circuit coupled to the correlator circuit.

18. **(Original)** The apparatus of claim 14 where said signal processor circuit includes a DSP.

19. **(Original)** The apparatus of claim 17, wherein the signal processor circuit averages correlation values over multiple time periods of the PN signals.

20. **(Original)** A receiver including two of the apparatus according to claim 14 that are operated in parallel.

21. **(Original)** The receiver of claim 20, wherein at least one correlator computes correlation values over a time period of less than one period of the PN signals and is used as an autonomous background correlator.

22. **(Original)** A method of tracking a CDMA pilot signal that comprises utilizing the apparatus of claim 14.

23. **(Original)** A method for tracking a CDMA pilot channel to discipline an oscillator, comprising:

downconverting the RF signal from the RF center frequency, f_{RF} to an intermediate center frequency of f_L, where f_L is greater than or equal to the CDMA chip rate, f_c, said downconversion incorporating bandpass filtering to remove extraneous signals while passing

said pilot channel signal;

converting signal format from analog to digital using a single analog-to-digital converter employing a sampling rate of f_s, to create the digital signal $\{s(n)\}$;

employing correlation to establish the correlation between $\{s(n)\}$ and locally generated versions of the I-channel and Q-channel PN signals, $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, respectively; and

generating an estimate of the frequency error of the oscillator using correlation values corresponding to (2M+1) time shifts of the locally generated versions of $\{I_{PN}(n)\}$ and $\{Q_{PN}(n)\}$, said time shifts being $K-\Delta_M$, $K-\Delta_{(M-1)}$, . . . , $K-\Delta_2$, $K-\Delta_1$, K, and $K+\Delta_1$, $K+\Delta_2$, . . . , $K+\Delta_{(M-1)}$, $K+\Delta_M$, where time shift of K corresponds to the time shift that provides the maximum correlation value, and the value of M is 4.

24. **(Currently Amended)** A method of tracking a pilot channel, comprising:

disciplining an oscillator ~~oscilator~~ including generating a spectrum shaped channel pilot signal $\{\gamma(n)\}$ from a chip-rate PN sequence $\{i(n)\}$ by:

oversampling the chip-rate PN sequence $\{i(n)\}$ at a higher sampling rate to yield a signal $\{a(n)\}$;

passing $\{a(n)\}$ through a first FIR filter whose impulse response coefficients are $\{g(n)\}$ to yield a signal $\{\beta(n\}$; and

filtering $\{\beta(n\}$ with a second FIR filter to yield the spectrum shaped channel pilot signal $\{\gamma(n)\}$.

25. **(Original)** The method of claim 24, wherein the spectrum shaped channel pilot signal $\{\gamma(n)\}$ is a spectrum shaped I-channel pilot signal.

26. **(Original)** The method of claim 24, wherein both positive overflows and negative overflows are monitored.

27. **(Original)** The method of claim 24, further comprising translating the spectrum shaped

I channel pilot signal $\{\gamma(n)\}$ down to a zero-offset-carrier frequency signal $\{s(n)\}$.

28. **(Original)** The method of claim 27, further comprising translating the zero-offset-carrier frequency signal $\{s(n)\}$ down to a baseband signal $\{w(n)\}$.

29. **(Original)** The method of claim 24, wherein a sampling clock is derived from a VCXO that is phase-locked to a reference frequency.

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30. **(Original)** The method of claim 24, wherein a correlation is computed at lags which are commensurate with a sampling rate.

31. **(Original)** The method of claim 24, wherein a matched filter is not employed.

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32. **(Original)** A receiver for performing the method of claim 24.

33. **(Currently Amended)** The method of claims 24, wherein the spectrum shaped channel pilot signal $\{\gamma(n)\}$ is a spectrum shaped Q-channel pilot signal.

34. **(Original)** An apparatus to track a pilot signal, comprising:

a correlator circuit adapted to oversample a chip-rate PN sequence $\{i(n)\}$ at a higher sampling rate to yield a signal $\{a(n)\}$, pass $\{a(n)\}$ through a first FIR filter whose impulse response coefficients are $\{g(n)\}$ to yield a signal $\{\beta(n\}$; and filter $\{\beta(n\}$ with a second FIR filter to yield a spectrum shaped pilot channel signal $\{\gamma(n)\}$.

35. **(Original)** The apparatus of claim 34, wherein said correlator circuit include a FPGA.

36. **(Original)** The apparatus of claim 34, further comprising:

a signal processor circuit coupled to the correlator circuit.

37. **(Original)** The apparatus of claim 34, wherein said signal processor circuit includes a DSP.

38. **(Original)** The apparatus of claim 36, further comprising an A/D converter coupled to said signal processor circuit.

39. **(Currently Amended)** The apparatus of claim ~~2~~34, wherein the first FIR filter includes a

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4-point FIR filter having all 4 coefficients at least substantially equal.

40. **(Currently Amended)** The apparatus of claim ~~2~~34, wherein the second FIR filter includes a 48-point FIR filter.

41. **(Currently Amended)** A method of tracking a CDMA pilot channel which comprises utilizing the apparatus of claim ~~2~~34.

42. **(Currently Amended)** The apparatus of claim ~~2~~34, further comprising an autonomous background correlator coupled to the correlator ~~correllater~~ circuit.

43. **(Currently Amended)** A receiver comprising at least two of the apparatus according to claim ~~2~~34.